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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

#6/A
Amdt

Application No.: 09/683,027
Applicant: Malinowski et al.
Filing Date: November 9, 2001
Title: **DUAL CHIP STACK METHOD FOR ELECTRO-STATIC DISCHARGE PROTECTION OF INTEGRATED CIRCUITS**

Atty. Docket: BUR9-2000-0228-US1
Today's Date: October 17, 2002
Examiner: Luan C. Thai
Group Art Unit: 2827
Fax: 703-872-9318

J. McMillan 10/28/02

Amendments Under 37 CFR 1.111

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Amendment A

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 19, 2002, Applicants respectfully request reconsideration of the outstanding rejection of claims in view of the amendments and remarks that follow. No fee is due by virtue of this amendment. However, if the PTO determines that a fee is required, please charge Applicants' Deposit Account, 09-0456.

CERTIFICATE OF MAILING

I hereby certify that, on the date shown below, this correspondence is being:

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☐ deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant commissioner of Patents, Washington, DC 20231.

Date: 10/18/2002

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ANTHONY J. CANALE
Name

Anthony J. Canale
Signature

Amend the application identified above as follows:

IN THE CLAIMS

Amend claims 1, 4, 8, 11, 12, 15, 19, 22, 23, 26, 30 and 33 as follows:

1. (Once Amended) An electronic device comprising:

a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, positioned in close proximity to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

A1

4. (Once Amended) An electronic device comprising:

a semiconductor chip including an integrated circuit; and

a non-semiconductor chip formed of an electrically insulating material, positioned in close proximity to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

A2

8. (Once Amended) An electronic device comprising:

a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, positioned in close proximity to said semiconductor chip, said non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, said first electrostatic discharge protection device electrically connected to said first electrostatic discharge sensitive device and said second electrostatic discharge protection device electrically connected to said second electrostatic discharge sensitive device.

A3

11. (Once Amended) The electronic device of claim 8, wherein:

said first electrostatic discharge sensitive device is selected from the group consisting of transistors, diodes, resistors, capacitors, and inductors;

said first electrostatic discharge protection devices is selected from the group consisting of spark gaps, field emission devices, diodes and gated diodes;

A4

said second electrostatic discharge sensitive device is selected from the group consisting of capacitors, resistors and inductors;

said second electrostatic discharge protection device is a spark gap or a field emission device; and

said spark gap, or field emission device, and at least a portion of said second electrostatic discharge sensitive device are integrally formed.

12. (Once Amended) An electronic device comprising:

a dual chip stack comprising:

a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, attached to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

Contd A4

15. (Once Amended) An electronic device comprising:

a dual chip stack comprising:

a semiconductor chip including an integrated circuit; and

a non-semiconductor chip formed of an electrically insulating material, attached to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

A5

19. (Once Amended) An electronic device comprising:

a dual chip stack comprising:

a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, positioned in close proximity to said semiconductor chip, said non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, said first electrostatic discharge protection device electrically connected to said first electrostatic discharge sensitive device and said second electrostatic discharge protection device electrically connected to said second electrostatic discharge sensitive device.

A6

22. (Once Amended) The electronic device of claim 19, wherein:

said first electrostatic discharge sensitive device is selected from the group consisting of transistors, diodes, resistors, capacitors, and inductors;

said first electrostatic discharge protection devices is selected from the group consisting of spark gaps, field emission devices, diodes and gated diodes;

A7

said second electrostatic discharge sensitive device is selected from the group consisting of capacitors, resistors and inductors;

said second electrostatic discharge protection device is a spark gap or a field emission device; and

said spark gap, or field emission device, and at least a portion of said second electrostatic discharge sensitive device are integrally formed.

23. (Once Amended) An electronic device comprising:

a dual chip stack mounted on a module, said dual chip stack comprising:

a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, attached to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

Cont'd A7

26. (Once Amended) An electronic device comprising:

a dual chip stack mounted on a module, said dual chip stack comprising:

a semiconductor chip including an integrated circuit; and

a non-semiconductor chip formed of an electrically insulating material, attached to said semiconductor chip, said non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, said electrostatic discharge protection device electrically connected to said electrostatic discharge sensitive device.

A8

30. (Once Amended) An electronic device comprising:

a dual chip stack mounted on a module, said dual chip stack comprising:

a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and

a non-semiconductor chip formed of an electrically insulating material, positioned in close proximity to said semiconductor chip, said non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, said first electrostatic discharge protection device electrically connected to said first electrostatic discharge sensitive device and said second electrostatic discharge protection device electrically connected to said second electrostatic discharge sensitive device.

#9

33. (Once Amended) The electronic device of claim 30, wherein:

said first electrostatic discharge sensitive device is selected from the group consisting of transistors, diodes, resistors, capacitors, and inductors;

said first electrostatic discharge protection devices is selected from the group consisting of spark gaps, field emission devices, diodes and gated diodes;

said second electrostatic discharge sensitive device is selected from the group consisting of capacitors, resistors and inductors;

said second electrostatic discharge protection device is a spark gap or a field emission device; and

said spark gap, or field emission device, and at least a portion of said second electrostatic discharge sensitive device are integrally formed.

#10

REMARKS

In the Claims

Claims 1, 4, 8, 11, 12, 15, 19, 22, 23, 26, 30 and 33 have been amended. No new matter has been added to the application by virtue of the present amendment.

Accordingly, claims 1-33 are pending in the subject application. It is respectfully requested that the pending claims 1-33 be reconsidered and passed to issuance in view of this response.

Claim Rejections – 35 U.S.C. 112, second paragraph

The Examiner has rejected claims 11, 22 and 33 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Applicants have made appropriate amendments to claims 11, 22 and 33 to provide the proper antecedent basis in the claims.

Therefore, Applicants respectfully submit that the rejections under 35 U.S.C. 112, second paragraph, have been overcome.

Claim Rejections – 35 U.S.C. 102 (e)

The Examiner has rejected claims 1, 2, 4, 5, 8, 9, 12, 13, 15, 16, 19, 20, 23, 24, 30 and 31 under 35 U.S.C. 102(e) as being anticipated by Lin (U.S. Patent No. 6,180,426).

Applicants have amended independent claims 1, 4, 8, 12, 15, 19, 23, 26, 30 to recite the limitation "... a non-semiconductor chip formed of an **electrically insulating material** ...". Support for Applicants' amendment can be found, for example, in paragraph [0044]. Applicants teach a non-semiconductor chip 120 formed of, for example, quartz. Quartz is known to those skilled in the art of semiconductor devices to be an electrically insulating material. Applicants' invention allows for passive devices such as an inductor to be optimized for ESD performance since the inductor is formed in an electrically insulating material so parasitic electrical currents are not formed in the non-semiconductor chip 120.

Lin does not anticipate or suggest Applicants' limitation of "... a non-semiconductor chip

formed of an **electrically insulating material** ...". Rather, Lin teaches first and second integrated circuit chips 305, 310 formed of a semiconductor material. Lin teaches that "... fabricating the second integrated circuit chip using its optimum semiconductor process ..." (column 3, lines 52-54); the internal circuits 365 formed on the second integrated circuit 310 "... may be DRAM, logic ..." (column 4, lines 28-29); and, that the second integrated circuit 310 is formed from "... dicing of the wafer ..." (column 5, line 24). Lin provides no teaching or suggestion of forming first or second integrated circuit chips 305, 310 from an electrically insulating material.

Claims 2, 5, 9, 13, 16, 20, 24, 27 and 31 are dependent upon independent claims 1, 4, 8, 12, 15, 19, 23, 26, 30, as amended, and, as discussed above, are not anticipated or suggested by Lin.

Therefore, Applicants respectfully submit that the rejections under 35 U.S.C. 102(e) have been overcome.

Claim Rejections – 35 U.S.C. 103 (a)

The Examiner has rejected claims 3, 6, 10, 14, 17, 21, 25, 28 and 32 under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Patent No. 6,180,426) in view of Voldman et al. (U.S. Patent No. 6,198,136); and, claims 7, 11, 18, 22, 29 and 33 under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Patent No. 6,180,426) in view of Staab et al. (U.S. Patent No. 5,610,790).

Claims 3, 6, 7, 10, 11, 14, 17, 18, 21, 22, 25, 28, 29, 32 and 33 are dependent upon independent claims 1, 4, 8, 12, 15, 19, 23, 26 and 30, as amended. As discussed above, Applicants believe that Lin neither teaches nor suggests Applicants' claims 1, 4, 8, 12, 15, 19, 23, 26 and 30, as amended. Thus, Lin in combination with Voldman et al. neither teach nor suggest Applicants' claims 3, 6, 10, 14, 17, 21, 25, 28 and 32. Likewise, Lin in combination with Staab et al. neither teach nor suggest Applicants' claims 7, 11, 18, 22, 29 and 33.

Therefore, Applicants respectfully submit that the rejections under 35 U.S.C. 103(a) have been overcome.

Attached hereto is a marked-up version of the changes made to the claims by the present amendment. The attachment is captioned "**Version with markings to show changes made**".

In light of the foregoing amendments and remarks, all of the claims now presented are believed to be in condition for allowance, and Applicants respectfully request that the outstanding rejections be withdrawn and this application be passed to issue at an early date.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully Submitted,

For: Malinowski et al.,

By: 

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